The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TSE-HUA LAN
and ZHUN ZHONG

Appeal No. 2004-1689
Application 09/912,132[1]

ON BRIEF

Before BARRETT, BLANKENSHIP, and NAPPI, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-12.

We reverse.

[1] Application for patent filed July 24, 2001, entitled "Reduced Complexity Video Decoding At Full Resolution Using Video Embedded Resizing."

BACKGROUND

The invention relates to video decoding with reduced computational complexity as stated in claim 1, reproduced below.

> 1. A method for decoding a video bitstream at a first resolution, comprising the steps of:
>
> producing residual error frames at a second lower resolution;
>
> producing motion compensated frames at the second lower resolution;
>
> combining the residual error frames with the motion compensated frames to produce video frames; and
>
> up-scaling the video frames to the first resolution.

THE REFERENCES

The examiner relies on the following references:

Choi	6,442,201	August 27, 2002 (filed August 5, 1998)
Campisano et al. (Campisano)	6,470,051	October 22, 2002 (filed January 25, 1999)
Vetro et al. (Vetro)	6,519,288	February 11, 2003 (filed March 6, 1998)

THE REJECTIONS

Claims 1-6 and 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi and Campisano.

Claims 7-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi and Campisano, further in view of Vetro.

We refer to the final rejection (Paper No. 9) (pages referred to as "FR__") and the examiner's answer (Paper No. 14) (pages referred to as "EA__") for a statement of the examiner's

rejection, and to the brief (Paper No. 13) (pages referred to as "Br__") for a statement of appellants' arguments thereagainst.

OPINION

The examiner finds that Choi discloses the subject matter of claim 1 except for the limitation of "up-scaling the video frames to the first resolution" (FR3). The examiner states (FR3): "Campisano teaches that once the decoding is done, the output to the display, shown in figure 5 item 92, can be up-sampled. Therefore, it would have been obvious to one of ordinary skill in the art, to up-scale to the higher resolution after decoding is done in order to get the desired picture quality."

Appellants argue that the combination of Choi and Campisano neither teaches nor suggests all of the claim limitations, in particular, "producing residual error frames at a second lower resolution" (Br5). It is argued that the examiner relies on the 4x8 IDCT unit in Fig. 5 of Choi, but that it is nowhere disclosed that the 4x8 IDCT unit produces residual error frames at a second lower resolution (Br5). It is argued that the decimation unit is placed after the adder 59 in Choi, and since the adder combines the outputs of the 4x8 IDCT unit 54 and the motion compensation unit 58, this implies that only the output frames of Choi are produced at a lower resolution and Choi cannot be reasonably interpreted as disclosing "producing residual error frames at a second lower resolution" (Br5).

The examiner states that "[a] careful review of figure 5, as well as column 7 lines 1-54 clearly shows that item 52 produces frames at a lower resolution by filtering the DCT's [sic, DCT coefficients] produced by the VLD and uses the filtered data which are analogous to residual error frames to do the motion compensation just as is claimed" (EA6).

We agree with the examiner that Choi teaches the steps of "producing residual error frames at a second lower resolution; producing motion compensated frames at the second lower resolution; combining the residual error frames with the motion compensated frames to produce video frames." "Residual error frames" are P and B frames. Choi discloses down-converting the high-resolution high definition (HD) signal to a lower resolution standard definition (SD) signal by horizontal and vertical down sampling after performing motion compensation (MC) at the full resolution (Fig. 2; col. 2, line 66, to col. 3, line 25). Choi then discloses down sampling the HD signal to half size through horizontal 1/2 down sampling, respectively scaling the motion vectors according to the reduced size, and performing the motion compensation with the scaled motion vectors (Figs. 3 and 4; col. 3, lines 26-67, especially lines 59-67), which meets the claim limitations. Figure 5 shows that all incoming frames are horizontally down sampled by elements 52 and 54 to a lower resolution and are motion compensated using scaled motion vectors

from motion vector scaling unit 56; the fact that P frames are further vertically down sampled in low pass filter and vertical decimation unit 71 is not precluded by the claim. Also, in Fig. 5 the B frames are further down converted by element 62 and motion compensation is performed by element 61 at a lower resolution, which also meets the claim limitations. However, the description at column 3 of Choi is the simplest to understand.

Appellants argue that there is no motivation to combine Choi with Campisano. It is argued that Choi is a down conversion decoding device that is used to convert a high definition (HD) signal to a lower resolution signal to be displayed on an NTSC type analog television and there would be no motivation to include the up-sampling of Campisano because then the frames could no longer be displayed on the lower resolution analog television, making Choi unfit for its intended purpose (Br4-5).

The examiner argues that the motivation to combine comes from the fact that both Choi and Campisano teach a need to have scalable decoders and "if a decoder manufacturer wanted to make a decoder that would display a picture on a low-resolution as well as a high-resolution monitor, it would build that capability into it" (EA5). The examiner notes that the decoding process was computationally intensive which is the reason the prior art discussed in Choi down sampled the picture data to perform the decoding process with more manageable amounts of data (EA5). The

examiner concludes that it would have been obvious "to add (not substitute as argued by the appellant in a previous action) an upscaling capability in order to assure that the decoder is universal to all monitors" (EA5-6).

We find that the applied prior art does not provide the necessary motivation for the proposed combination. The invention is performing motion compensation of residual error (B and P) frames at a lower resolution and then up-scaling the video frames to the original resolution, which reduces the overall computational complexity of the decoding. We agree with the examiner that Choi expressly teaches performing motion compensation on residual error frames of reduced resolution to reduce computational and hardware complexity at column 3, lines 18-67. However, we agree with appellant that there is no motivation in Choi to up-scale the video frames to their original resolution because the whole purpose of Choi is to reduce HD signals to SD signals. Thus, we look to see whether Campisano provides the necessary motivation.

The examiner relies on the up-sampling unit 92 in Fig. 5. However, we must look at the whole of Campisano. Campisano discloses decode systems "which allow selective scaling of video presentation by a predetermined reduction factor, while at the same time allowing for reduced external memory requirements for frame buffer storage" (col. 1, lines 39-43). Campisano has a

normal video mode and a scaled video mode. In a normal video mode, the frame buffer has three buffer areas for receiving full size I, P, and B frames and in a scaled video mode the frame buffer has five buffer areas, a first and second are for receiving full size I and P frames and third, fourth, and fifth areas for receiving scaled I, P, and B frames (e.g., col. 3, lines 20-35; Fig. 6; col. 9, lines 31-33). Decoding and motion compensation is performed on full resolution frames from an MPEG input source by video decoder 54 and I and P pictures stored in the memory buffer (col. 9, lines 47-67; col. 12, lines 14-16). Decoded full-size macroblocks are received by the decimation unit 82 where they may or may not be scaled and stored in the frame buffers (col. 10, lines 46-54). Thus, Campisano does not disclose performing motion compensation on a reduced resolution frame. We next examine the up-scaling teachings of Campisano.

In a normal mode, decimation unit 82 outputs decoded data full-size macroblocks to memory control unit 52 for storage in frame buffers 53 (col. 10, lines 49-51) with B-coded pictures preferably being decimated (col. 10, lines 4-8). In the scaling mode, decimation unit 82 scales the full-size macroblocks and outputs full-size macroblocks for I and P frames and scaled macroblocks for I, P, and B frames to memory control unit 52 for storage in frame buffers 53 (col. 10, lines 51-54). The frames in the two modes are shown in Fig. 6. In the normal display

mode, full-size scan lines are retrieved from the buffer storage 53 and fed through the decimation unit 82 where B frames are re-expanded for display and the other scan lines for I and P frames are unchanged (col. 10, line 60, to col. 11, line 5). It appears from the arrow from 82 to 84 that the full-size scan lines are fed into the scan line video buffers 84 and then to vertical and horizontal up-sample logic 94. In a scaling display mode, scaled scan lines are retrieved from frame buffer storage 53 and fed into scan line video buffers 84 to vertical and horizontal up-sample logic 94 (col. 11, lines 6-12). "Upsample controls are received from display fetch unit 92, which coordinates letterbox formatting, SIF upsampling, 4:2:0 to 4:2:2 upsampling, and flicker reduction (in accordance with the principles of the above-incorporated [U.S. Patent 5,973,740])." (Col. 11, lines 12-17). (Note the control line from unit 92 to up-sample logic 94.) It appears that up-sampling is performed for both normal (full-size) and scaled lines. As explained in U.S. Patent 5,973,740 ('740 patent), referred to by its application number in Campisano, up-sampling might be to change material that is encoded in a 16:9 aspect ratio into a conventional 4:3 aspect ratio by expanding in a 12:16 rate ('740 patent, col. 12, line 62, to col. 13, line 2; col. 13, lines 17-18). A 4:3 aspect ratio can be converted to a 16:9 aspect ratio by down-sampling the vertical samples by 3/4 ('740

patent, col. 10, lines 29-33), i.e., 4(4/4): 3(3/4) = 16:9, so the process can be reversed by up-sampling the vertical by 4/3. The color difference blocks can also be up-sampled, e.g., from 4:2:0 to 4:2:2. However, while there is up-sampling in Campisano, it is only to change the aspect ratio and not to up-sample the resolution "to the first resolution" as required by all of the independent claims 1 and 10-12. There is no motivation in Campisano to up-scale back to a first resolution. Accordingly, we conclude that the examiner has failed to establish a prima facie case of obviousness as to the independent claims. Vetro does not cure the deficiencies of Choi and Campisano with respect to the rejection of the independent claims. Therefore, the rejection of claims 1-12 is reversed.

REVERSED

LEE E. BARRETT
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

ROBERT E. NAPPI
Administrative Patent Judge

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